Proximity rapid thermal diffusion for emitter formation in silicon solar cells

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Abstract

Results are presented for emitters formed by the proximity rapid thermal diffusion (PRTD) process for silicon solar cells. Diffusion temperature and diffusion atmosphere are investigated as parameters for varying the emitter profile and concentration. Junction depth is approximated by ball grooving and staining to delineate the junction and examination under optical microscopy. Sheet resistance measurements are carried out by four point probe to assess doping concentration and uniformity. Ellipsometry measurements are used to monitor the oxide thickness formed during the doping process. Current-voltage profiles are used to assess the electronic properties and conversion efficiency of complete devices under 1.5AM(G) illumination.

Introduction

The formation of a doped emitter is a fundamental process in the production of silicon solar cells and is a well-established field. Conventional solar cell emitters are typically on the order of 1-2 µm thick and in the majority of cases are formed by diffusion of dopant impurities such as phosphorus, arsenic and boron.

Textured and structured thin silicon solar devices such as micro and nano pillar cells offer the potential for significant material savings over thick wafer and polysilicon devices but demand much tighter control of emitter parameters to prevent carrier depletion in small scale features.

Typically, emitters for structured devices are required to be highly doped and shallow. Emitters produced by spin on dopant (SOD) sources in conjunction with rapid thermal processing (RTP) permit fine control over junction depth and dopant concentration but it is a non-trivial matter to apply a conformal layer to non-uniform surfaces.

A variation on this technique, proximity rapid thermal diffusion (PRTD), sees the SOD applied to a sacrificial source wafer which is placed in proximity to samples to be doped. When heated, mass diffusion of the dopant from the SOD layer results, this is transported in the gas phase to the surface of the samples to be doped where adsorption and diffusion occurs [1].

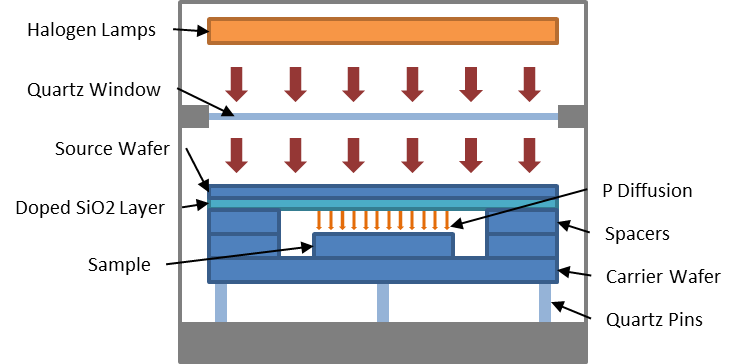
By controlling the diffusion time and temperature it is possible to accurately control junction depths and dopant profiles whilst achieving homogeneity of doping, even on textured and structured surfaces [2].

This paper presents results for PRTD diffused emitters in planar silicon solar cells. This process is being developed as a technique to form radial junction micro-pillar solar cells.

**Experimental**

As supplied p-type <111> silicon wafers were subjected to a piranha clean process (3:1 – H2SO4:H2O2) to remove organic contamination followed by de-ionised water rinse and nitrogen drying.

An SOD solution (supplied by Filmtronics) consisting of phosphorus pentoxide (P2O5) and silicon dioxide (SiO2) in a solvent carrier was applied to the wafer and spun at 1000 rpm for 30 seconds to produce a uniform film. The wafer was then baked at 200 °C for 30 minutes to drive off residual solvent and leave a P2O5 containing SiO2 film on the surface. When necessary the SOD solution was diluted with Methanol (CH3OH) to vary the phosphorus concentration.



*Fig 1. Equipment configuration for proximity rapid thermal diffusion*

Samples to be diffused were prepared from 675µm thick <100> silicon wafers with resistivity of 0.1-0.5 Ω/cm cleaved into 13mm2 samples. Prior to processing they were subjected to a piranha etch process, water rinse process and N2 drying. These were then loaded into the RTP system on top of a silicon carrier wafer. Spacers consisting of pieces of silicon wafer were placed around the edge of the carrier before the source wafer was placed atop these to complete the diffusion stack (Fig 1).

After loading, samples were subjected to a variety of diffusion processes with temperature varied in the range 770 °C – 1030 °C and oxygen (O2) content in the nitrogen (N2) process gas varied in the range 0-10 %.

Typical thermal cycles for diffusions consisted of a 60 second ramp to the peak diffusion temperature followed by a 15 minute hold. At the end of the hold the temperature was ramped down to 500 °C over 3 minutes to improve reorganisation of the diffused phosphorous in the silicon lattice and reduce defects.

Results and Discussion

Four point probe measurements were used to map the sheet resistance of as diffused devices. The standard deviations of the measurements were used to assess the uniformity of the doping process and are plotted on graphs as error bars.

Additionally the oxide layer deposited on the surface during the diffusion process was measured by ellipsometry to investigate the effect of the various parameters on its formation.

To analyse the depth of the junction produced, ball grooving and staining was used. This technique consists of forming a groove in the doped silicon substrate using a steel ball coated with a diamond paste. The milled groove is shallow but must exceed that of the junction depth such that both the emitter and underlying substrate are exposed.

A staining solution consisting of hydrofluoric acid, chromium trioxide and de-ionised water is then applied which creates a visible contrast difference between the two regions. The contrast results because the silicon etch rate is dependent on the dopant type and concentration. By measuring the radii of the two differentiated regions, combined with the known radius of the steel ball, the junction depth is expressed by:

|  |  |
| --- | --- |
|  | (1) |

where xj is the depth of the junction, R is the ball radius, a is the radius of the larger ring and b the radius of the smaller ring.

*Fig 2. Effect of diffusion temperature on sheet resistance and junction depth with 90% N2 / 10% O2 atmosphere*

The effect of diffusion temperature is plotted in Fig 2 with a significant decrease in sheet resistance between 770 °C and 870 °C. This results predominantly from the exponential effect of temperature on diffusivity of impurities in silicon. A smaller increase occurs between 870 °C and 970 °C as the solid solubility limit of phosphorus in silicon is approached [3]. Above 970 °C there is virtually no change in the sheet resistance despite a large increase in junction depth. This suggests that the surface dopant concentration, which dominates sheet resistance, has reached equilibrium with the impurity concentration available from the source during diffusion. This assumption is further supported by a lack of further reduction in sheet resistance with increased temperature despite an increase in solid solubility and resulting ability of the substrate to take up more dopant.

Approximations for peak doping concentration based on sheet resistance and junction depth suggest an increase from 1.7E+20 atoms/cm3 to 2.9E+20 atoms/cm3 between 870 °C and 970 °C. The value for peak concentration at 970 °C is approaching the electronic activity limit for phosphorus diffused in silicon which indicates that higher temperatures will only serve to increase the junction diffusion rate and have minimal effect on sheet resistance. This is in agreement with the results shown in Fig 2 for a temperature increase from 970 °C to 1030 °C.

A nominally exponential increase in junction depth with temperature can also be observed which is in agreement with the exponential relationship between diffusivity and temperature exhibited by phosphorus in silicon.

*Fig 3. Effect of oxygen concentration on sheet resistance and grown oxide thickness for 870 °C 15 minute diffusion*

The addition of O2 to the N2 carrier gas has a significant effect on both the average sheet resistance of diffused samples and the uniformity of the emitter (Fig 3). Under pure N2, sheet resistances in excess of 300 Ω/□ were typical with standard deviation values exceeding 30. The addition of 2.5 % O2 reduced both the sheet resistance and standard deviation by an order of magnitude. Further increases in O2 had negligible effect on the sheet resistance but did further improve the standard deviation from 3.5 to 1.5. A high level of uniformity is particularly important when diffusing a conformal emitter into structured devices. Also notable is the approximately eight fold increase in the oxide thickness grown on the surface of the devices to be doped when diffused under O2. Whilst this does not agree with conventional oxide growth theory, oxide formation by RTP has been shown to yield much higher oxidation rates compared to conventional furnaces [4]. The enhanced oxide formation may also account for the deep junctions and high peak doping concentrations achieved at relatively low temperatures which do not agree with conventional diffusion theory. It has been shown that phosphorus diffusivity is significantly enhanced in the presence of a growing oxide. This is believed to be due to the enhanced silicon self-interstitial formation under oxidation conditions and an associated increase in interstitial dopant diffusion, the primary means of phosphorus transport in silicon, which results [5].

To assess the electronic performance of various emitters, a selection of diffused samples were first MESA etch edge isolated. Subsequently a 1µm layer of aluminium was sputtered onto the rear side to form an ohmic contact to the p-type wafer. Front side contacting to the n-type emitter was achieved by sequentially evaporating bi-layer nickel-silver (15nm and 1000nm thick respectively) dots of 1.5mm diameter around the edge of the front surface. Typically a grid contact arrangement would be applied to a planar device to minimise series resistance, however, the process is ultimately to be applied to arrays of micro-pillars for which a grid contacting scheme would be incompatible. It is noted that the use of the current contacting scheme is likely a contributory factor to the relatively limited performance exhibited by devices. This issue may subsequently be resolved by use of a transparent conductive oxide which would be compatible with both planar and structured devices.

*Fig 5. J-V measurements for various diffusion temperatures*

Devices were tested under AM1.5(G) illumination using a class A solar simulator and a Keithley 2400 Sourcemeter to sweep and measure voltage and current respectively. A selection of J-V curves are shown in Fig 5.

*Fig 6. Efficiency and Jsc data for various diffusion temperatures*

The J-V curves for 870 °C and 970 °C show an improvement in fill factor (FF) from 37.73 % to 53.73 % with increasing temperature. This is accredited to the improving charge separation with increasing doping concentration.

At 1030 °C there is a significant loss in current generation and efficiency (Fig 6) despite a broadly similar FF (56.9 %) and calculated peak doping concentration. It is believed that the highly doped and deeply diffused emitter is causing significant carrier recombination and reducing effective current generation. It has been shown by simulation that, with regard to highly doped emitters, shallower junctions should perform better [6].

*Fig 7. Comparison of 970 °C 15 minute diffusion process, a PC1D model of the as diffused emitter and the improvement attainable with a shallow diffusion of the same profile.*

To assess the effect of shallow emitters with regard to the doping technique under investigation, a PC1D model which reproduces the results found for the 970 °C 15 minute diffusion was prepared (Fig 7). Values for parasitic resistances were extracted from the measured device data and the emitter profile was modelled based on sheet resistance and junction depth. Values for carrier lifetime were approximated based on the doping concentration in each region whilst those for recombination at the front surface were deliberately set to imitate a highly doped, poorly passivated emitter. The reflectance of the device was based on measured reflectance data. By decreasing the junction depth to 250 nm it was possible to improve the modelled efficiency from 4.83 % to 6.35 % with an increase of Isc from 12.8 mA to 16.7 mA. This suggests a significant enhancement in performance may be attained by modifying the diffusion process to attain a shallower emitter. Further enhancements are possible with contacting and passivation improvements.

**Conclusions**

Emitters have been formed in p-type silicon with good uniformity and high peak doping concentration by proximity rapid thermal diffusion. High diffusion rates are achievable for relatively low temperatures (< 1000 °C) with the addition of O2 to the N2 diffusion atmosphere.

Solar cells have been prepared from the diffused samples to assess their performance with peak efficiencies of 4.83 %. Modelling has indicated that efficiencies can initially be significantly improved by reducing the diffused junction depth. Devices in their current state possess high series resistance and high recombination rates amongst other factors which inhibit their peak output.

Further work will focus on reducing the junction depth and minimising other performance limiting factors. Such refinements should improve efficiency and result in a diffusion process suitable for application to micro-pillar devices which require shallow and highly doped emitters.

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